ABSTRACT OF THE DISCLOSURE

On a semiconductor substrate, a well is formed. In the well, one MOS transistor including a gate electrode, a source region, a source field limiting layer and a source/drain region, and another MOS transistor including a gate electrode, a drain electrode, a drain field limiting layer and a source/drain region are formed. The one and another MOS transistors are connected in series through the source/drain region common to the two transistors. Accordingly, a semiconductor device can be provided in which increase in pattern layout area is suppressed when elements including a high-breakdown voltage MOS transistor are to be connected in series.